Schedule 1

Project Plan

1. Statement of Work

1.1 Objectives:

To co-develop with Huawei, the GaN Amplifier device with **target specifications** as follows. IME will work with Huawei to design and run 2 iterations before confirming the final specifications mutually.

NO.	Parameter	requirement	Description
Performance			
1	Frequency	0.4~3.0GHz	
2	P1dB	150W	Minimum
3	Drain Efficiency	70%@P1dB	Minimum
4	Gain	400~700MHz: 22dB 0.7~2.2GHz: 20dB 2.3~2.7GHz: 18dB	Minimum
5	Input return loss	-10dB	maximum
6	IMD	?	maximum
Dynamic characteristics			
7	Ciss	20 pF	maximum
8	Crss	2 pF	maximum
9	Coss	30 pF	maximum
10	Gain varation over temperature	0.01dB/℃	maximum
11	P1dB varation over temperature	0.005dB/℃	maximum
12	Operating Drain Voltage	28V, 40V, 50V	Optional
13	Input impedance	2 ohm	minimum
14	Output impedance	2 ohm	minimum
Working Ratings			
15	Storage Temperature	-65~150℃	
16	Operating Junction	200℃	

	Temperature		
17	Breakdown Voltage	65V, 28V operation 90V, 40V operation 120V,50V operation	
18	Capable of handing	10:1VSWR, 5dB overdirve	
ESD protection characteristics			
19	Integrated ESD protection		
20	Human Body Model(per JESD22-A114)		1A (minimum)
	Machine Model(per EIA/JESD22-A115)		A (minimum)
	Charge Device Model(per JESD22-C101)		IV (minimum)

1.2 Responsibilities:

IME and Huawei shall be jointly responsible for the establishment of specifications for each of the 3 planned runs (see scopes).

IME shall be responsible for the circuits design and modeling of the GaN devices.

IME shall be responsible for the fabrication of the designed devices.

IME and Huawei shall be jointly responsible for the measurements and characterizations of the fabricated chips.

1.3 Scope:

WP#	Work Package	Description
1	Device Simulation/Design	• Simulate epitaxial layer GaN on silicon for HEMT structure • Simulate key HEMT device characteristics including threshold voltage, breakdown voltage, output current, transconductance, • Design passive structures for characterization • Tapeout design layout
2	Device Fabrication	• Develop necessary process modules • Integrate process modules into final fabrication

3	Active and Passive Device Characterization	• Take DC and RF measurements of active and passive devices • Compare to simulations • Refine simulation parameters based on characterization results • Identify areas for fabrication improvement based on measurement results
4	Fabrication Improvement	• Improve layout design based on characterization • Use characterization data for process improvement • Complete new fabrication flow
5	Models Developed from Device Characterization	• Take measurement data and implement in ADS • Fit data to HEMT templates • Fit data for passive devices including inductors, capacitors, resistors, and transmission lines
6	Circuit Design 1	• Literature Review • Circuit Specifications • Block Design and Simulation • Refine Specifications • Transistor Level Design and Simulation • Layout • Post-Layout Optimization • Tapeout
7	Circuit Fabrication 1	• Complete fabrication based on device integration flow
8	Circuit Characterization 1	• DC Characteristics • RF Characteristics • Compare Experiments with Simulations • Model Refinement based on Measurements
9	Circuit Design 2	• Refine Specifications • Design Optimization based on Refined Model • Layout • Post-Layout Optimization • Tapeout
10	Circuit Fabrication 2	• Complete fabrication based on device integration flow
11	Circuit Characterization 2	• DC Characteristics • RF Characteristics • Compare Experiments with Simulations • Deliver to Prototype to Huawei

2. Project Schedule / Time Frame

(An indication of the project schedules, time frames and milestones, etc. may be put in a tabulated format for easy reference), e.g.

	2012				2013				2014			
Work Packages	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
1. Device Simulation/Design												
2. Device Fabrication												
3. Active and Passive Device Characterization												
4. Fabrication Improvement												
5. Models Developed from Device Characterization												
6. Circuit Design 1												
7. Circuit Fabrication 1												
8. Circuit Characterization 1												
9. Circuit Design 2												
10. Circuit Fabrication 2												
11. Circuit Characterization 2												

3. Deliverables

(A restatement of the deliverables indicated in para 2 and 3. This is to clearly state what RI and Coy expect at the end of the project. Should also include reporting requirements)

e.g. The deliverables for this project are:

I. xxxxx
2. xxx
3. xxxxxx

4. Project Development Fees and Payment Schedule

Total Development Fees charged by IME after taking into consideration in-kind contributions from Coy: S$XXXXX.

1st Payment upon PO, XX% of the total Development Fees (i.e., S$XXX)

2nd Payment upon full delivery milestone, XX% of the total Development Fees (i.e., S$XXX)

5. Project Milestones

1st Milestone: GDS sent by XXX
2nd ...

...
Full Delivery Milestone: Delivered chips to XXX